What is claimed is:

1. A method of producing a timing signal having a predetermined time interval, comprising the steps of:

initiating a ramping timing signal having a predetermined duration and setting a timer latch output signal substantially simultaneously in response to an occurrence of an input signal;

enabling counting of a predetermined number of clock signals in response to said occurrence of said input signal;

pausing said ramping timing signal at a present value upon an occurrence of a first clock cycle following said enabling of counting;

restarting said ramping timing signal when said predetermined number of clock cycles has occurred; and

resetting said timer latch output signal upon an expiration of a predetermined duration of said ramping timing signal;

wherein said timer latch output signal is said timing signal.

2. The method of claim 1, wherein said predetermined time interval is substantially equal to the sum of said predetermined duration of said ramping timing signal and a time interval encompassing said predetermined number of clock cycles.

3. The method of claim 2, wherein said step of enabling counting includes the step of resolving a meta-stability condition by clocking said input signal with said clock signal.

4. A timer circuit, comprising:

a ramp timer responsive to an input signal for generating a ramp signal and providing an end of ramp signal at an output when said ramp signal attains a predetermined amplitude;

a counter responsive to a clock signal for counting a predetermined number of clock cycles, said input signal causing an enabling of said counter to count said cycles of said clock signal;

a timer control circuit for pausing said ramp signal of said ramp timer upon an occurrence of a first clock cycle following said enabling of said counter, and for restarting said ramp signal upon an occurrence of a last one of said predetermined number of clock cycles counted by said counter; and

a timer latch circuit for providing an output timing signal, wherein said output timing signal of said timer latch is set by said input signal and reset by said end of ramp signal.

5. The timer circuit of claim 4, wherein said ramp timer comprises:

a first input for receiving said input signal;

a second input for receiving a ramp timing control signal; and

an output for providing said end of ramp signal;

wherein said ramp timer is further adapted to receive a pause signal and a restart signal from said timer control circuit.

6. The timer circuit of claim 4, wherein said counter comprises:

a first input for receiving an enable signal;

a second input for receiving a counter timing control signal;

a third input for receiving a clock signal; and

an output for providing a terminal count signal to said timer control circuit.

7. The timer circuit of claim 4, wherein said timer latch comprises:

a first input for receiving an input signal;

a second input for receiving the end of ramp signal from said ramp timer; and

an output for providing an output timing signal,

wherein said timer latch circuit comprises a D flip flop.

8. The timer circuit of claim 4, wherein said ramp timer comprises:

a ramp generator circuit for providing said ramp signal;

a comparator for providing said end of ramp signal; and

a settable reference voltage source.

9. The timer circuit of claim 4, further including a meta-stability resolving circuit interposed between said input and said counter for receiving said input signal, clocking said input signal with said clock signal, and applying said clocked input signal to said counter to enable said counter to count.

10. The timer circuit of claim 9, wherein said meta-stability circuit comprises a pair of series connected D flip flop circuits for applying said input signal to said counter in response to said clock signal.

11. A timer circuit comprising:

means for generating a ramp timing signal, said ramp timing signal being initiated upon an occurrence of an input signal;

means for counting a predetermined number of clock cycles, said occurrence of said input signal causing an enabling of said means for counting;

means for pausing said ramp timing signal upon the occurrence of a first clock cycle following said enabling of said means for counting, and for restarting said ramp timing signal upon an occurrence of a last one of said predetermined number of clock cycles counted by said means for counting;

means for generating a signal denoting an end of ramp timing signal; and

means for receiving said input signal and said end of ramp timing signal and providing an output timing signal in response thereto.

12. A glitch trigger circuit, comprising:

a timer circuit, comprising;

a ramp timer responsive to an input signal for generating a ramp signal and providing an end of ramp signal at an output;

a counter responsive to a clock signal for counting a predetermined number of clock cycles, said input signal causing an enabling of said counter;

a timer control circuit for pausing said ramp signal of said ramp timer upon the occurrence of a first clock cycle following said enabling of said counter, and for restarting said ramp signal from a level attained when said ramp signal was paused upon an occurrence of a last one of said predetermined number of clock cycles counted by said counter; and

a timer latch circuit for providing an output timing signal having a predetermined duration;

and

a D flip-flop circuit responsive to said output timing signal for providing a trigger output signal if said input signal exhibits a pulse width less than said duration of said output timing signal.

13.. The glitch trigger circuit of claim 12, wherein said timer circuit further includes a meta-stability resolving circuit interposed between said input and said counter for receiving said input signal, clocking said input signal with said clock signal, and applying said clocked input signal to said counter to enable said counter to count.

14. The glitch trigger circuit of claim 13, wherein said meta-stability circuit comprises a pair of series connected D flip flop circuits for applying said input signal to said counter in response to said clock signal

15. A glitch trigger filter, comprising:

a timer circuit, comprising:

a ramp timer for generating a ramp signal and providing an end of ramp signal at an output;

a counter responsive to a clock signal for counting a predetermined number of clock cycles, said input signal causing an enabling of said counter;

a timer control circuit for pausing said ramp signal of said ramp timer upon the occurrence of a first clock cycle following said enabling of said counter, and for restarting the ramp signal upon an occurrence of a last one of said predetermined number of clock cycles counted by said counter; and

a timer latch for providing an output timing signal;

and

a D flip-flop circuit responsive to said output timing signal for providing a trigger output signal if said input signal exhibits a pulse width greater than said duration of said output timing signal.

16. The glitch trigger filter of claim 15, wherein said timer circuit further includes a meta-stability resolving circuit interposed between said input and said counter for receiving said input signal, clocking said input signal with said clock signal, and applying said clocked input signal to said counter to enable said counter to count.

17. The glitch trigger filter of claim 16, wherein said meta-stability circuit comprises a pair of series connected D flip flop circuits for applying said input signal to said counter in response to said clock signal

18. A trigger hold-off timer circuit, comprising:

a timer circuit, comprising:

a ramp timer for generating a ramp signal and for providing an end of ramp signal at an output;

a counter responsive to a clock signal for counting a predetermined number of clock cycles, said input signal causing an enabling of said counter;

a timer control circuit for pausing the ramp signal of said ramp timer upon the occurrence of a first clock cycle following said enabling of said counter, and for restarting said ramp signal upon an occurrence of a last one of said predetermined number of clock cycles counted by said counter; and

a timer latch circuit for providing a hold-off output signal to a first flip-flop circuit for maintaining a logic level of said first flip-flop for a predetermined time interval;

said first flip-flop circuit asserting an Accepted Trigger signal; and

a second flip-flop circuit for producing an output signal in response to said Accepted Trigger signal to provide a control input to said timer circuit.

19. The trigger hold-off timer circuit of claim 18, wherein said hold-off output signal produced by said timer latch is applied to said first flip-flop circuit to maintain said first flip-flop circuit at a logic low level for said duration of said predetermined time interval.

20. The trigger hold-off timer circuit of claim 18, wherein said first flip-flop and said second flip-flop comprise D flip-flops.

21. The trigger holdoff timer circuit of claim 18, wherein said timer circuit further includes a meta-stability resolving circuit interposed between said input and said counter for receiving said input signal, clocking said input signal with said clock signal, and applying said clocked input signal to said counter to enable said counter to count.

22. The trigger holdoff timer circuit of claim 21, wherein said meta-stability circuit comprises a pair of series connected D flip flop circuits for applying said input signal to said counter in response to said clock signal

23. A timer circuit, comprising:

a ramp timer responsive to an input signal for generating a ramp signal and providing an end of ramp signal;

a counter responsive to a clock signal for counting a predetermined number of clock cycles, said input signal causing an enabling of said counter;

a timer control circuit for pausing the ramp signal of said continuous timer at a level upon the occurrence of a first clock cycle following said enabling of said counter, and for restarting the ramp signal from said level upon an occurrence of a last one of said predetermined number of clock cycles counted by said counter; and

a logic gate for combining said input signal and said end of ramp signal for providing an output timing signal.

24. The timer circuit of claim 23, wherein said logic gate comprises an AND logic gate.

25. The timer circuit of claim 24, wherein said timer circuit further includes a meta-stability resolving circuit interposed between said input and said counter for receiving said input signal, clocking said input signal with said clock signal, and applying said clocked input signal to said counter to enable said counter to count.

26. The timer circuit of claim 25, wherein said meta-stability circuit comprises a pair of series connected D flip flop circuits for applying said input signal to said counter in response to said clock signal.